In the Specification:

Please replace the paragraph beginning at page 3, line 10, with the following amended paragraph:

-- The goal of the most common approaches to modifying mask patterns, whether it be rules-based or model-based, is to ensure the layout patterns are replicated within the specifications assumed by the circuit designer. In some cases, efforts have been made to ensure that the patterns are reproduced over the largest possible lithographic process window (i.e., range of dose and defocus). However, this approach still results in deficiencies in producing circuit patterns. Circuit layout follows a set of design rules that specify limits and allowed ranges of pattern dimensions. Due to the strong desire to provide the smallest chip dimensions possible, certain minimum geometries might be allowed in the design rules even though they may not be optimum to achieve the highest yield. Quite frequently the particular layout chosen is dictated by convenience rather than optimum yield or space restriction. Minimum geometries are chosen due to limitations in the automated layout generators rather than space restrictions. Thus, it is highly desirable to eliminate such yield limiting geometries wherever they are not absolutely required. --

Please replace the paragraph beginning at page 4, line12, with the following amended paragraph:

-- In accordance with the present invention, yield-based optimization of layout design parameters is employed in model-based OPC. Model-based OPC systems employ an iterative optimization process wherein simulated image contour placement is compared to the edge placement of the original design pattern, and feedback corrections are made until a satisfactory match is found. In accordance with the present invention, the image contours are evaluated for a set of sampling points located on the original design, along with the image contours of associated sampling points that relate to process-identified yield factors. The term 'associated' is intended to indicate that each

sampling point has associated with it, a set of additional sampling points. The associated sampling points are required since the yield functions use variables such as the width of a line, the width of a space, distance to a contact or other interlayout conditions. Since these variables are related to distances, more than one point in the design is required. These same variables are used to define a merit function embodied in yield functions derived from process information, such as, yield as a function of linewidth and space between lines, or interlayer layout conditions. --

Please replace the paragraph beginning at page 10, line 3, with the following amended paragraph:

-- Again, with reference to Figure 1, the process in accordance with the present invention begins in conventional manner with the step of creating and storing a design ~~a~~ mask pattern equal to the design layout, as shown by "set Mask = desired layout" in block 1. An existing OPC tool then runs a simulation on the mask pattern and predicts what the actual wafer pattern image would be after optical projection onto the wafer substrate. The predicted wafer pattern image is then stored, as shown by block 3. Sampling points along the predicted wafer pattern image edge are then defined and set, as shown by the step of block 5. In this regard, sampling points may be selected in accordance with the degree of change in the pattern layout and where layout features are prone to failure. For example, where the pattern changes rapidly, more samples may be taken than where straight lines are involved. Where a standard OPC process is employed, the position of the sampling points on the predicted wafer pattern image edge are compared to the position of corresponding points on the design mask pattern image edge. If the position of the two points is within some predetermined range of one another, sampling of this point terminates. Thus, the merit function here is solely based upon the distance between the two points being within a certain specified tolerance of one another. --

Please replace the paragraph beginning at page 12, line 19 with the following amended paragraph:

-- For further description, reference is made to the layout according to Figure 3 and the flow diagram of Figure 1, starting with block 9. In the initial steps of the algorithm, sampling points (step of block 5) have been picked, as shown at points 1, 2, 3 and 4 along the design width lines. The set of associated sampling points for point 1 includes point 3 and 2 defining the width of the space and the width of the line (step of block 7). It is assumed that the new edge placements have been calculated, i.e., points 63, 57 ~~59~~, 61 and 65 are known based on the mask layout (lines 47). It is also assumed that the quality of the edge placement for point 1 is being evaluated. As shown in Figure 3, the merit function is a function of the linewidth (distance between points 63 and 57) and the space (distance between points 57 and 61). Since we are looking at point 1, the algorithm has to decide whether or not the current position of point 57 is optimum (or close to optimum) in terms of yield. This question is answered by looking at the yield function as a function of d_edge1. For this particular iteration d_edge2, d_edge3, d_edge4 are all known and are kept fixed. Therefore the yield function depicted in Figure 2 can be converted to a merit function of d_edge1 only which is schematically shown in Figure 3a. The question the process of Figure 1 addresses is; how close is the predicted edge placement d_edge1 to the edge placement which would result in maximum yield? This question is addressed in steps shown by blocks 9, 10, 11 and 13 in Figure 1. The step of block 9 determines the positions of the predicted line edge at the various sampling points in the process, such as sampling point 57 in Figure 3. Then, in the steps of block 11, the value of the variables from the associated sampling points and the related merit function is calculated. In this regard, block 11 references a "modified merit function". This term is used to distinguish the process in accordance with the present invention from that of the conventional OPC process wherein the merit function is merely one of distance. --

Please replace the paragraph beginning at page 18, line 11, with the following amended paragraph:

-- Figure 7 shows a common layout pattern where a gate line crosses over active area. The possible failures here may be due, for example, to reflectivity mechanisms due to underlying substrate effects. As shown, gate 77 crosses an active area 79 which may be subject to reflectivity variations caused by an underlying substrate. This may result in an undesirable linewidth variation affecting gate performance. As can be seen, the same sampling approach as used in Figure 3 may be used here over the linewidth of the gate. Thus, the variables for each sampling point would involve the edge placement error of the gate and the distance to the edge of the active area ~~RX~~. The yield curves for such conditions are shown in Figure 8. In this configuration, it is assumed that a difference in height is present at the boundary between active area and surrounding oxide. In a typical gate process, this step would be covered by the gate stack upon which an anti reflective material and resist is coated during the gate lithography process. The planarization properties of the organic coatings used, lead to reflective notching of the gate at some distance from the boundary between active area and oxide. This distance is plotted on the y-axis of Figure 8. Yield in this arrangement is determined by the capability to maintain the desired gatewidth within a certain typically very narrow tolerance. In order to maintain optimum yield, a counteractive widening of the gatewidth at a distance of approximately 200nm from the edge is required to maintain optimum yield, as shown in Figure 8. --